REMARKS

This application contains claims 1-30. Claims 2, 3, 11, 12, 20, 21 and 23 have been amended. No new matter has been introduced. Reconsideration is respectfully requested.

Claims 2, 3, 11, 12, 21 and 23 were rejected under 35 U.S.C. 112, second paragraph, for use of the term "substantially." Applicant has amended these claims to remove the term.

Claims 1-4, 6-8, 10-17, 20-24 and 26-29 were rejected under 35 U.S.C. 102(b) over Fallside et al. (U.S. Patent 6,326,806). Applicant respectfully traverses the rejection of claims 1-4, 6-8 and 10-17. Claim 20 has been amended to clarify the distinction of the claimed invention over the cited art.

Fallside describes a FPGA-based communications access point, which includes a physical interface circuit (PHY), a storage element, and a configuration control circuit (abstract). The configuration control circuit provides an initial configuration bitstream to the FPGA at power-up (col. 3, lines 62-64). The FPGA then interfaces with a communications channel via the PHY (col. 4, lines 1-4). The FPGA may subsequently be reconfigured by downloading a configuration bitstream via the communication channel and storing the configuration bitstream in the storage element, which may be a local RAM or other memory (col. 4, lines 14-20, and col. 5, lines 40-45). After the configuration bitstream has been received and stored in the storage element, the FPGA is reconfigured by loading the new configuration bitstream from the local memory into the FPGA (col. 5, lines 49-52).

Claim 1 recites network node apparatus comprising a PHY device and a field-programmable logic device, which has two ports: a configuration port for receiving program

code in order to program the logic device, and a data input port for receiving communication data. Both the configuration port and the data input port are coupled to the PHY device. Thus, the apparatus of claim 1 is capable of receiving and loading program code into the field-programmable logic device directly from a network via the PHY device, without requiring an additional storage element and configuration control circuit as in Fallside.

The FPGAs shown in all of Fallside's embodiments (Figs. 1, 3 and 5) each include only a single port that is coupled to the PHY. Fallside's FPGAs are programmed by receiving the configuration bitstream through another port, which is coupled to the RAM or other storage element in the access point. Fallside neither teaches nor suggests that the FPGA could be programmed through a port that is coupled to the PHY as recited in claim 1.

Thus, the Examiner has not met the requirements for an anticipation rejection that are set forth in MPEP 2131:

> TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California* ,814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)… "The identical invention must be shown in as complete detail as is contained in the… claim." *Richardson v. Suzuki Motor Co* ., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Specifically, the Examiner has not identified the elements in Fallside that are equivalent to the configuration port and data input port of claim 1. Had the Examiner done so, it would have been clear that

Fallside does not meet the explicit requirement of claim 1 that both the configuration port and the data input port be coupled to the data output port of the PHY device.

Therefore, claim 1 is patentable over the cited art. In view of the patentability of claim 1, dependent claims 2-4 and 6-8 are also believed to be patentable.

Independent claim 10 recites apparatus for communication over a network, comprising a code server and a network node. The network node comprises a PHY device and a field programmable logic device, which comprises a configuration port and a data input port, both of which are coupled to the data output port of the PHY device, as in claim 1. The Examiner rejected claim 10 on the same grounds as claim 1. As explained above, however, Fallside does not teach or suggest that both the configuration port and the data input port be coupled to the data output port of the PHY device.

Therefore, claim 10 is patentable over the cited art for the reasons stated above in regard to claim 1. In view of the patentability of claim 10, dependent claims 11-17 are also believed to be patentable.

Independent claim 20 recites a method for network communication in which a node receives signals from a communication network, and the signals are processed at the node to generate a digital data output. The claim has been amended to clarify the structure of the node by reciting, as in claims 1 and 10, that the digital data output is generated at a data output port of a PHY device in the node. The node comprises a programmable processor, which has a configuration port and a data input port, both of which are coupled to the data output port of the PHY device, as in claims 1 and 10. As explained above, Fallside neither teaches nor suggests this structural feature.

Thus, claim 20, as amended, is patentable over the cited art. In view of the patentability of claim 20, dependent claims 21-24 and 26-29 are also believed to be patentable.

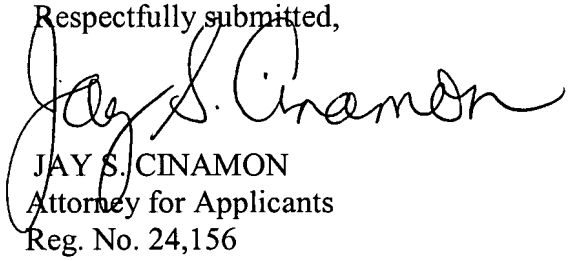
Furthermore, notwithstanding the patentability of the independent claims in this application, the dependent claims also recite independently-patentable subject matter. For example, claims 2, 11 and 21 as amended, recite the added limitation that the apparatus or network node comprises no non-volatile memory for holding the program code. In the grounds of rejection of these claims (page 3, second paragraph, in the Official Action), the Examiner actually confirmed the novelty of the claims, by stating (correctly) that "Fallside teaches the apparatus comprises volatile memory for holding the program code," i.e., RAM 208, or storage element 108 in Fig. 1. Thus, claim 2 is clearly patentable over the cited art.

Similar arguments may be made regarding the other dependent claims, but they are omitted here for the sake of brevity.

Claims 5, 9, 18, 19, 25 and 30 were rejected under 35 U.S.C. 103(a) over Fallside in view of Magal et al. (U.S. Patent 6,933,745) or Mantey et al. (U.S. Patent 6,918,027). Applicant respectfully traverses these rejections. In view of the patentability of independent claims 1, 10 and 20, as explained above, dependent claims 5, 9, 18, 19, 25 and 30 are also believed to be patentable.

Applicant believes the amendments and remarks presented hereinabove to be fully responsive to all of the grounds of rejection raised by the Examiner. In view of these amendments and remarks, Applicant respectfully submits that all of the claims in the present application are in order for allowance. Notice to this effect is hereby requested.

Respectfully submitted,



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